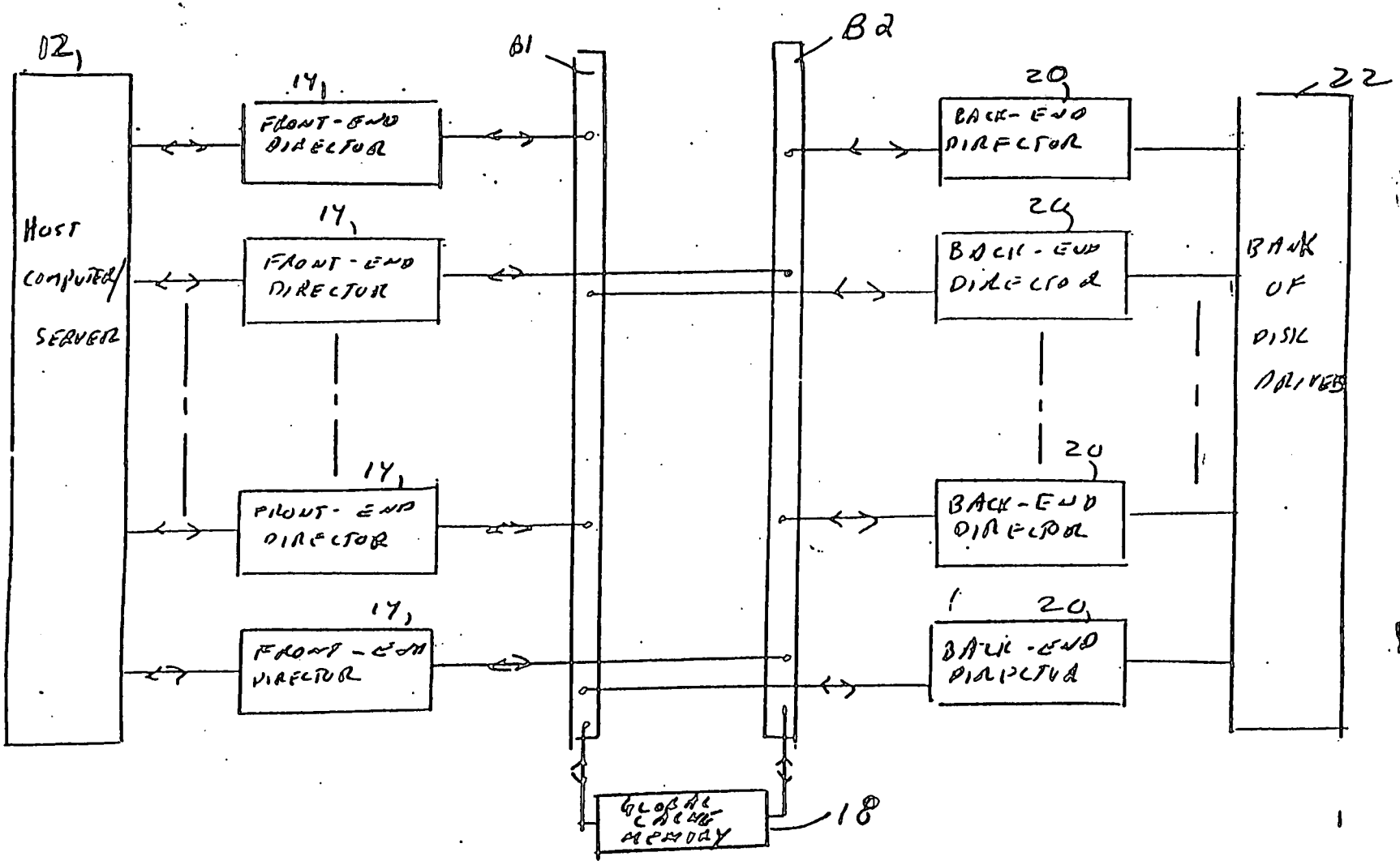
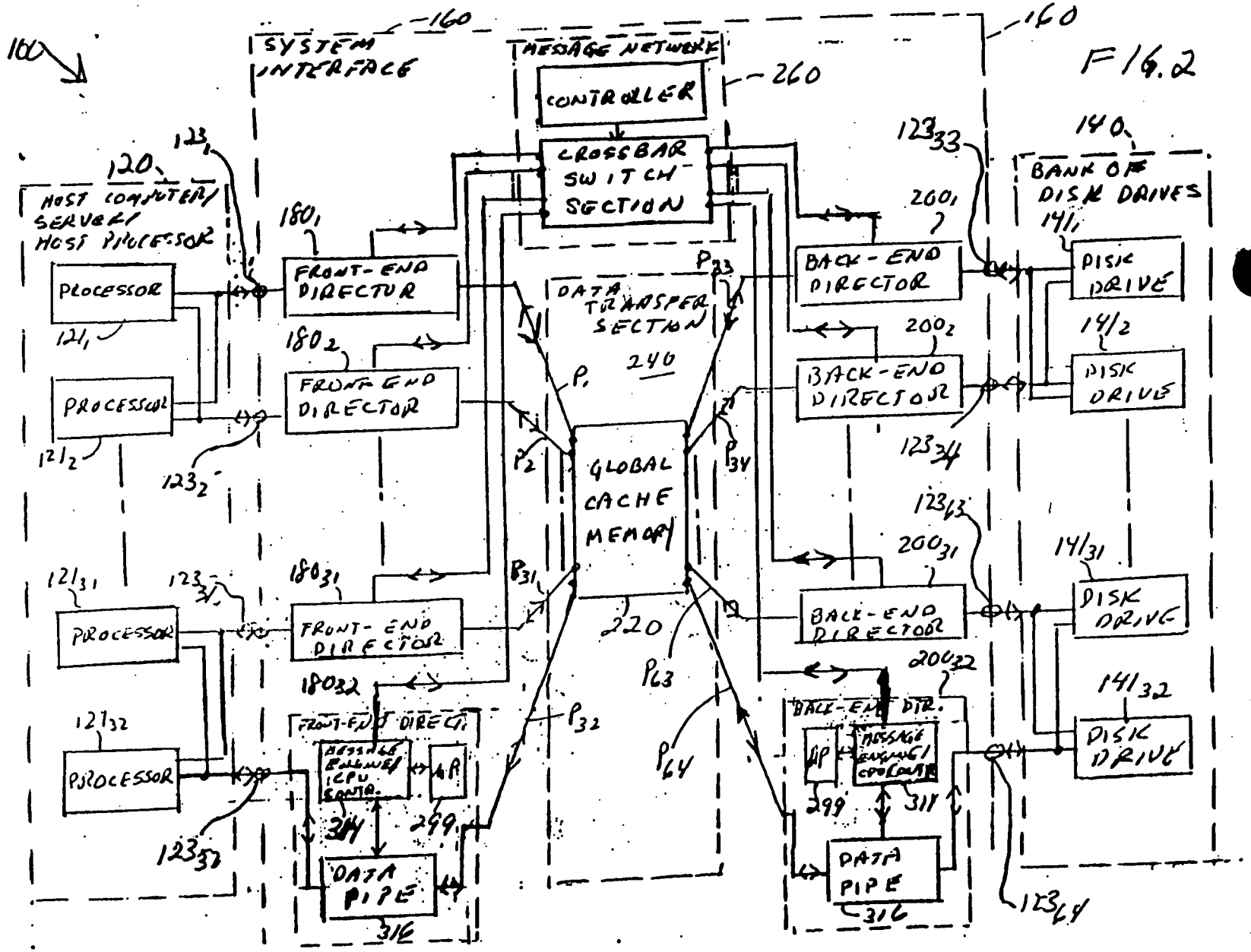
FIG. 1
PRIOR ART





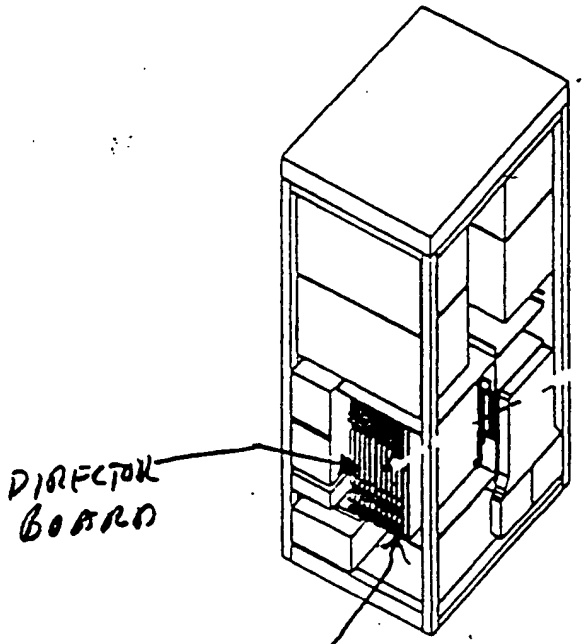
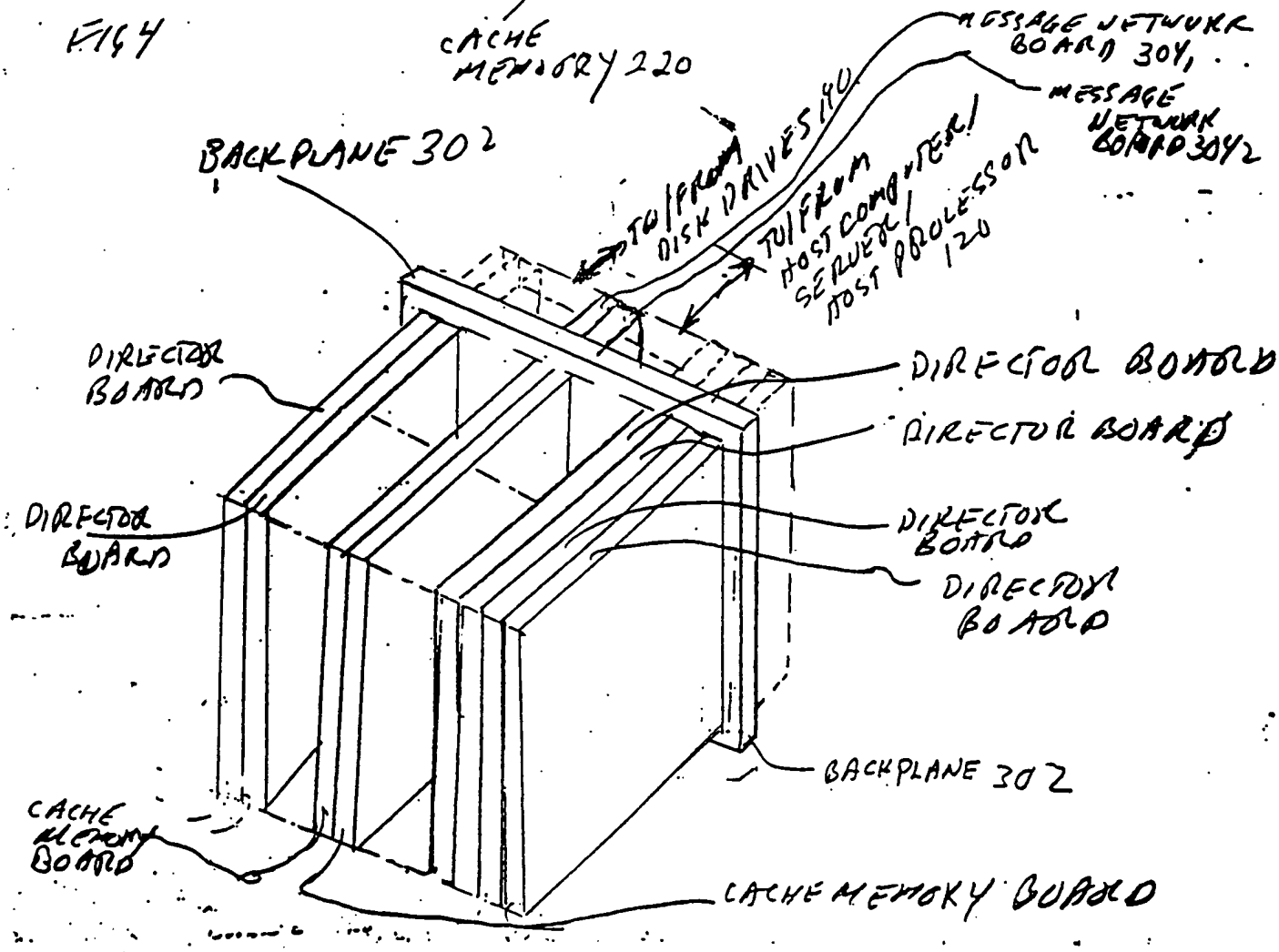


FIG. 3

FIG 4



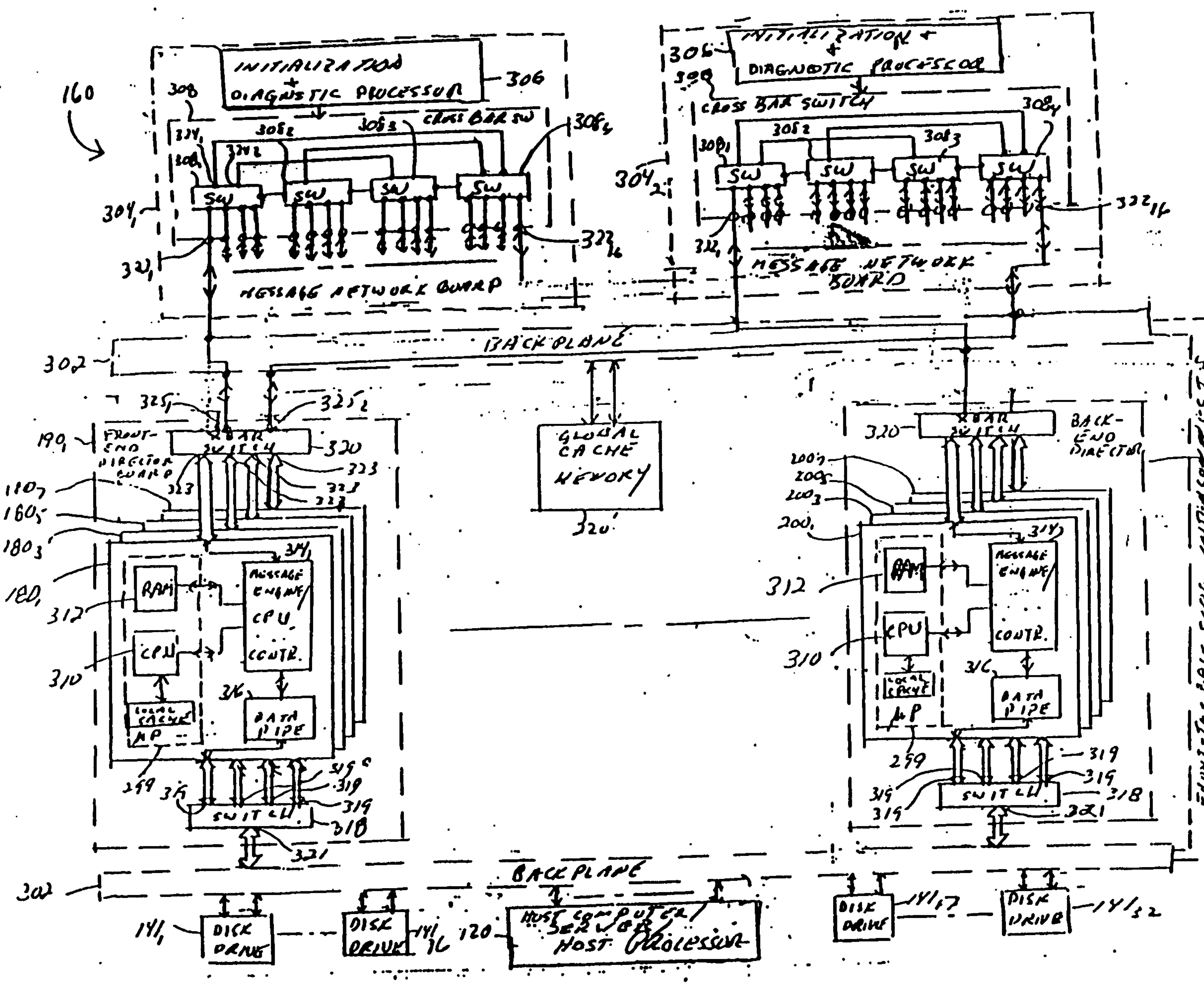

160
INITIALIZATION + DIAGNOSTIC PROCESSOR
306
308
CROSS BAR SW
SW
MESSAGE NETWORK BOARD
INITIALIZATION + DIAGNOSTIC PROCESSOR
CROSS BAR SWITCH
BACKPLANE
302
XBAR SWITCH
320
FRONT-END DIRECTOR BOARD
GLOBAL CACHE MEMORY
BACK-END DIRECTOR
MESSAGE ENGINE
CPU
CONTR.
RAM
LOCAL CACHE
μP
DATA PIPE
SWITCH
318
321
FRONT-TO-BACK SIDE INTERCONNECT
BACKPLANE
DISK DRIVE
HOST COMPUTER/ SERVER/ HOST PROCESSOR
120

FIG 5

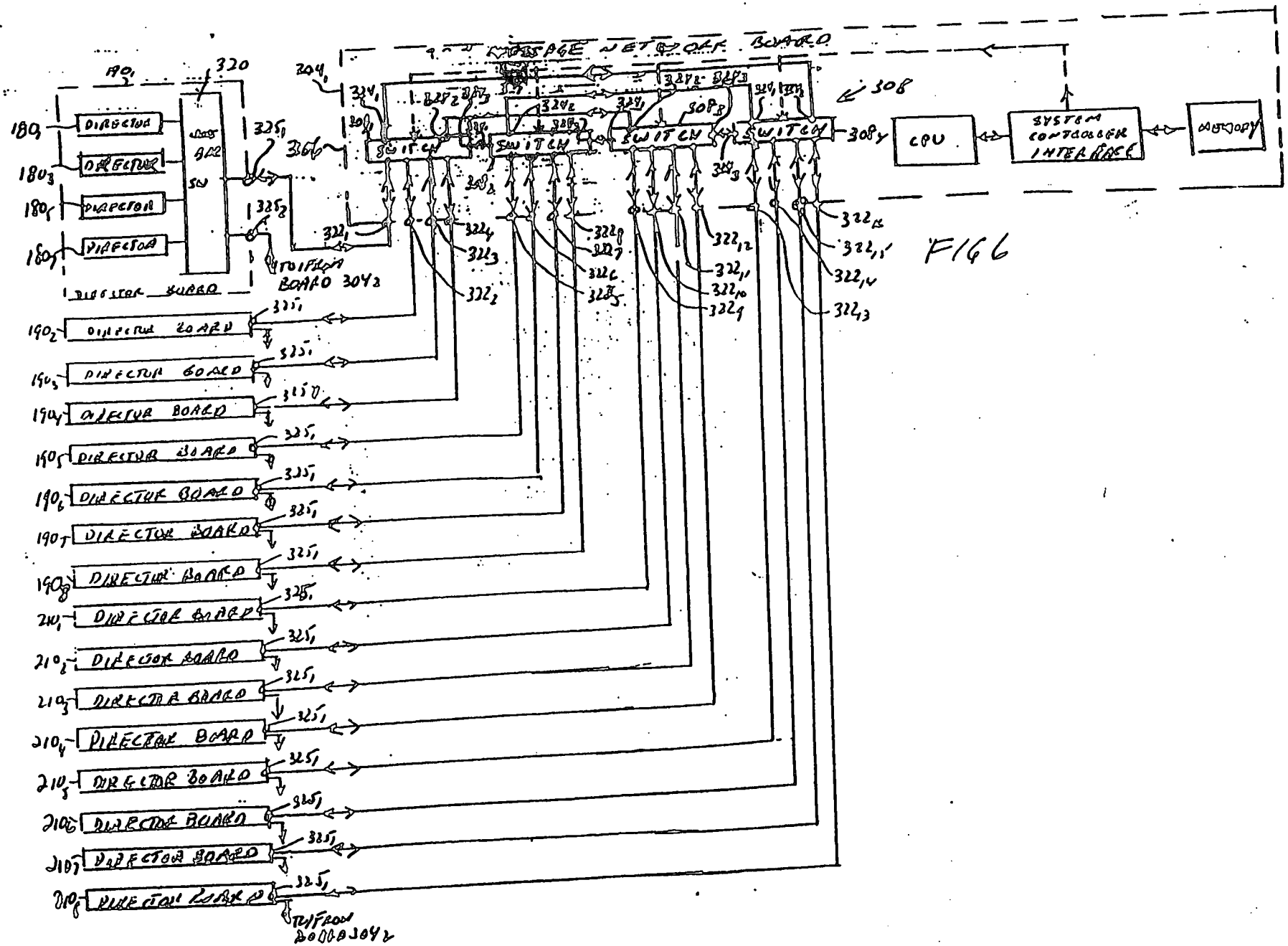

SWITCH
CPU
SYSTEM CONTROLLER INTERFACE
MEMORY
DIRECTOR BOARD
TO/FROM BOARD 304₂

FIG 6

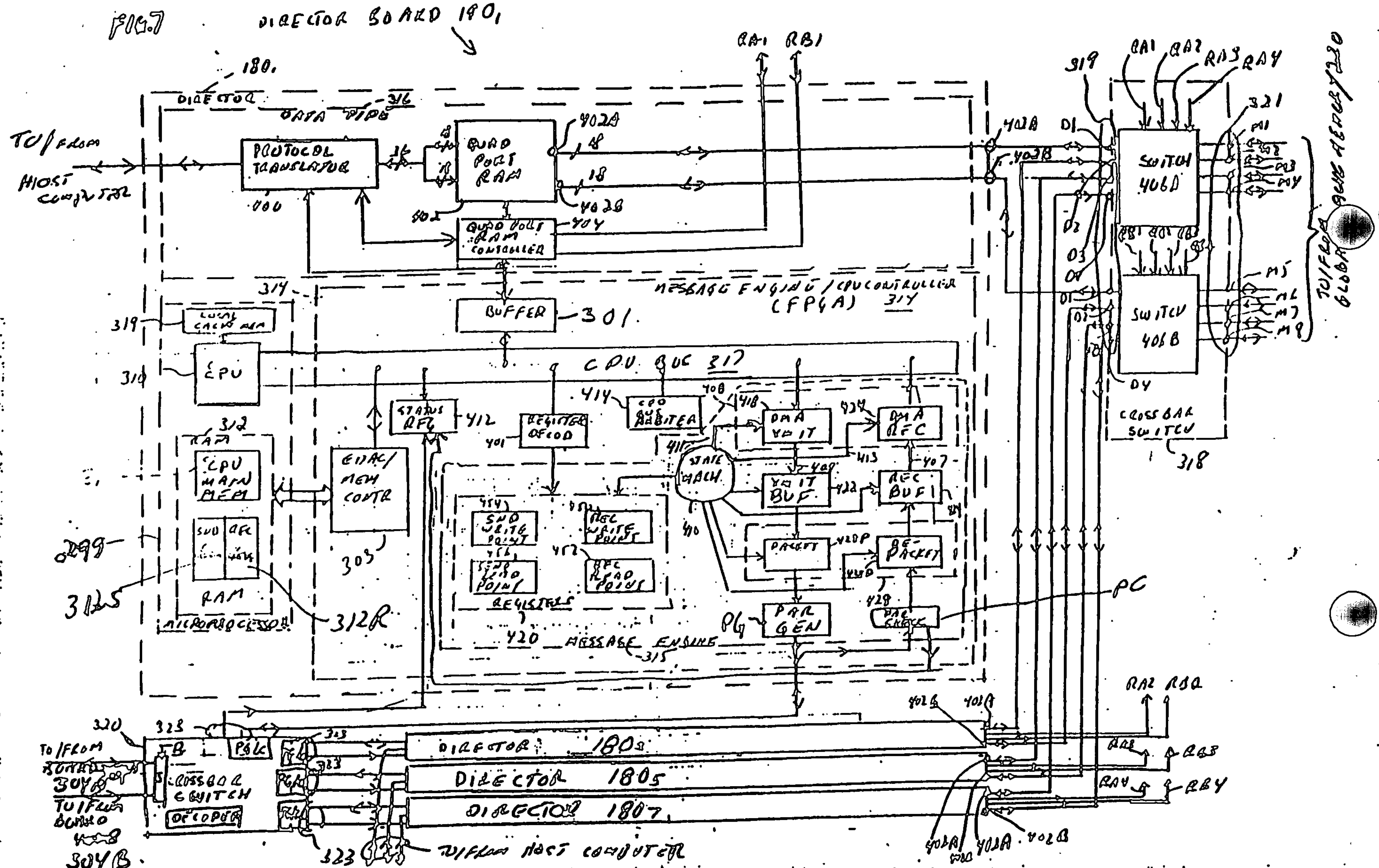

DIRECTOR BOARD 180₁
DIRECTOR
180₁
DATA PIPE 316
TO/FROM HOST COMPUTER
PROTOCOL TRANSLATOR
400
QUAD PORT RAM
402
402A
402B
QUAD PORT RAM CONTROLLER
404
RA1 RB1
MESSAGE ENGINE/CPU CONTROLLER (FPGA) 314
BUFFER 301
LOCAL CACHE MEM
CPU
CPU BUS 317
STATUS REG
412
REGISTER DECOD
401
EDAC/MEM CONTR
303
CPU BUS ARBITER
414
DMA XMIT
DMA REC
XMIT BUF
REC BUF
STATE MACH
410
PACKET
RE-PACKET
PAR GEN
PAR CHECK
PG
PC
REGISTERS
420
MESSAGE ENGINE 315
CPU MAIN MEM
RAM
MICROPROCESSOR
299
312R
SWITCH 406A
SWITCH 406B
CROSS BAR SWITCH 318
TO/FROM GLOBAL CACHE MEMORY 220
RA2 RB2
RA3 RB3
RA4 RB4
DIRECTOR 180₃
DIRECTOR 180₅
DIRECTOR 180₇
CROSSBAR SWITCH
DECODER
TO/FROM HOST COMPUTER
TO/FROM BOARD 304A
TO/FROM BOARD 304B
323
320

FIG.7

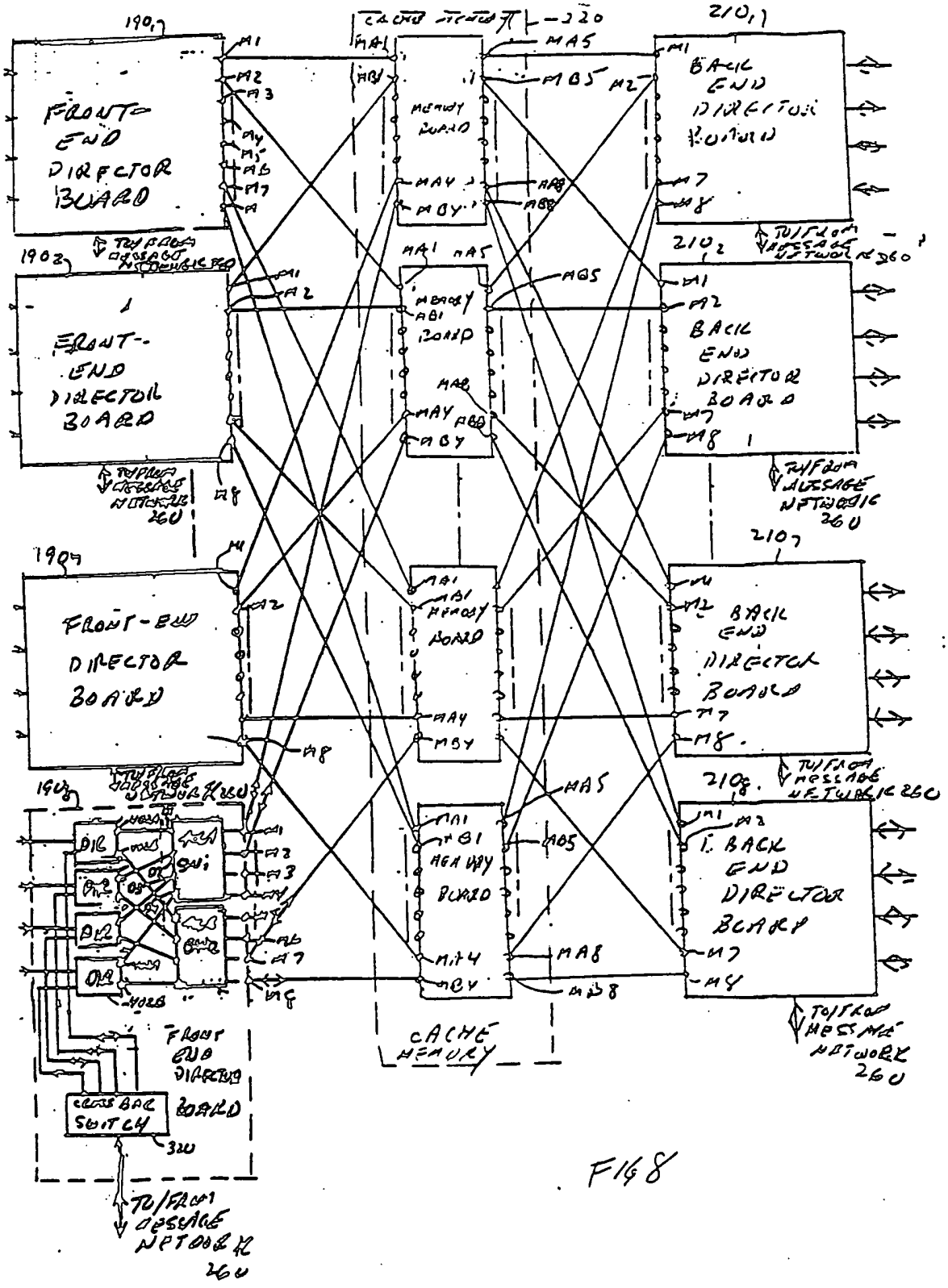
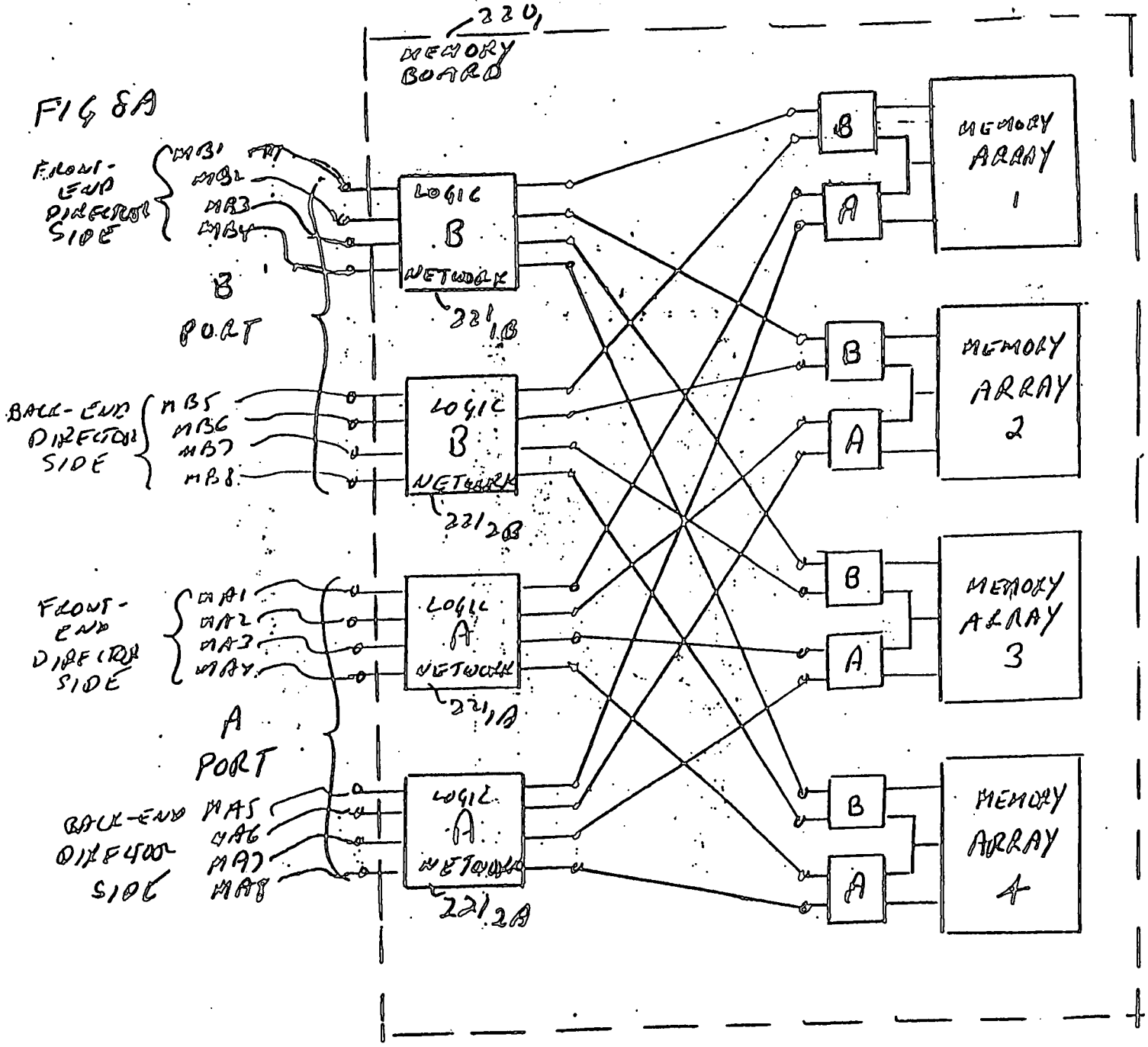

FRONT-END DIRECTOR BOARD
FRONT-END DIRECTOR BOARD
FRONT-END DIRECTOR BOARD
FRONT-END DIRECTOR BOARD
MEMORY BOARD
MEMORY BOARD
MEMORY BOARD
MEMORY BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
CACHE MEMORY
CROSS BAR SWITCH
TO/FROM MESSAGE NETWORK 26U

FIG 8

FIG 8A



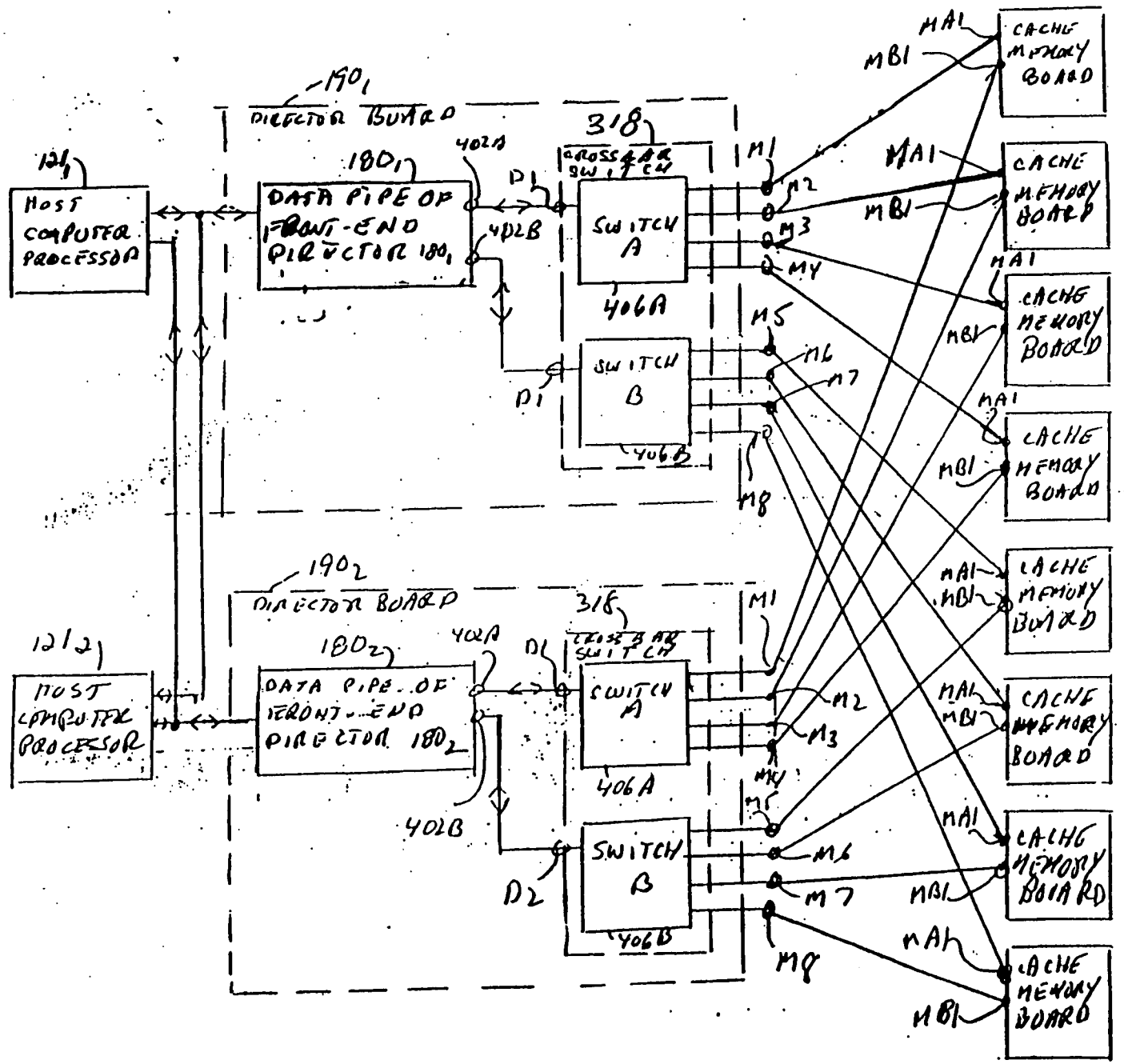

HOST COMPUTER PROCESSOR
121
DIRECTOR BOARD
190
DATA PIPE OF FRONT-END DIRECTOR
180
402A
402B
D1
D2
318
CROSS BAR SWITCH
SWITCH A
SWITCH B
406A
406B
M1
M2
M3
M4
M5
M6
M7
M8
MA1
MB1
CACHE MEMORY BOARD

FIG 8B

FIG. 8C

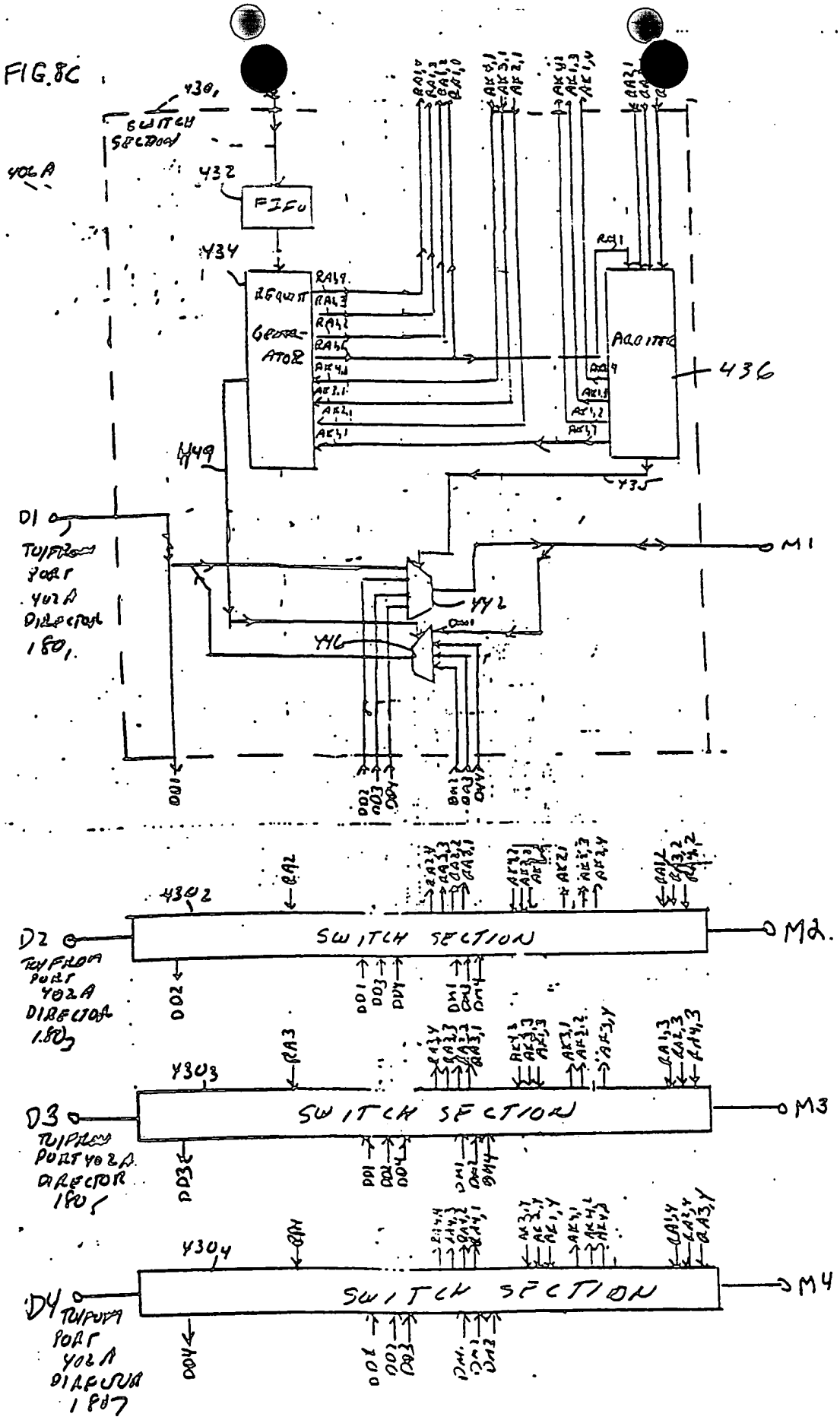

SWITCH SECTION
FIFO
ARBITER
436
M1
M2
M3
M4
SWITCH SECTION
SWITCH SECTION
SWITCH SECTION

FIG 9

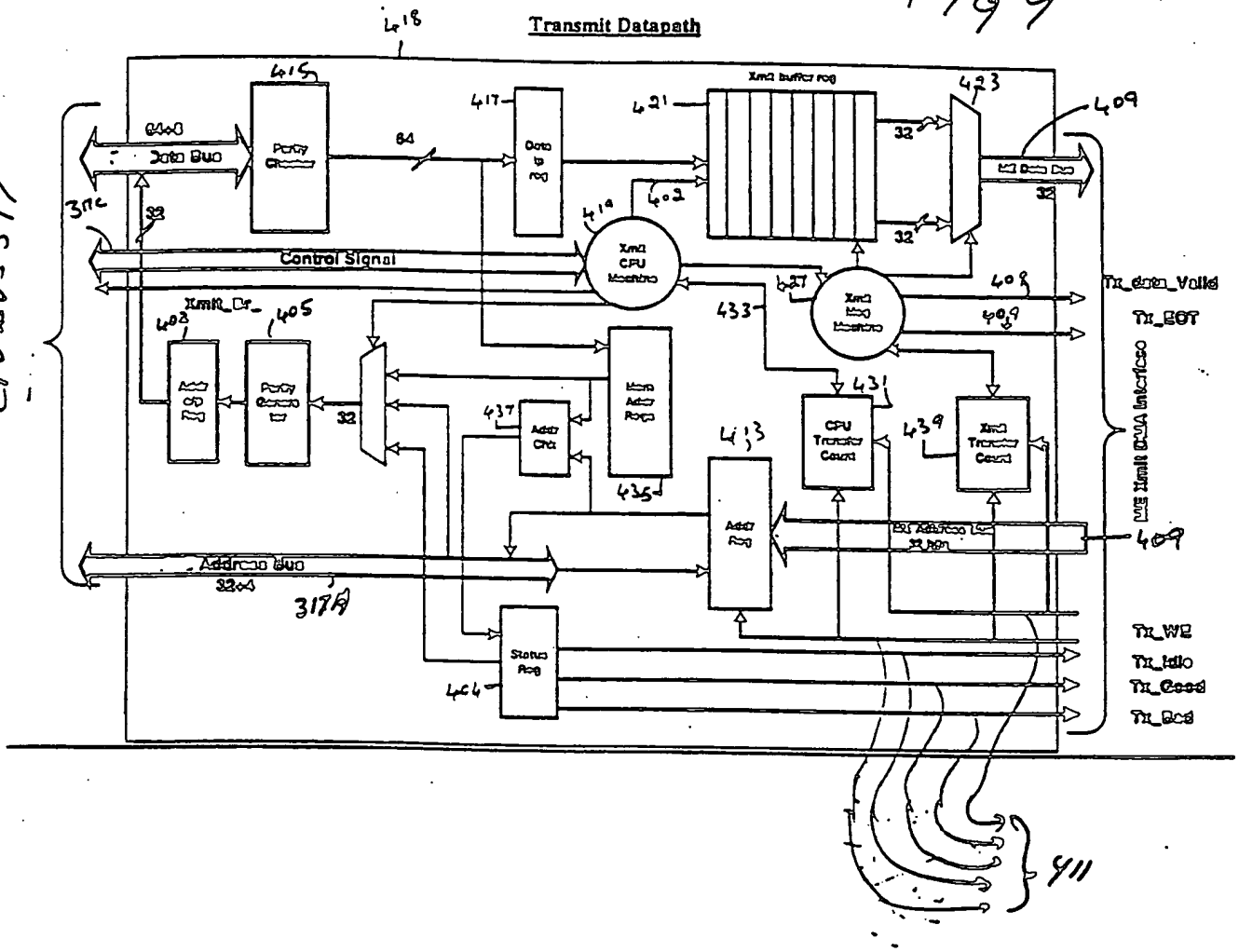
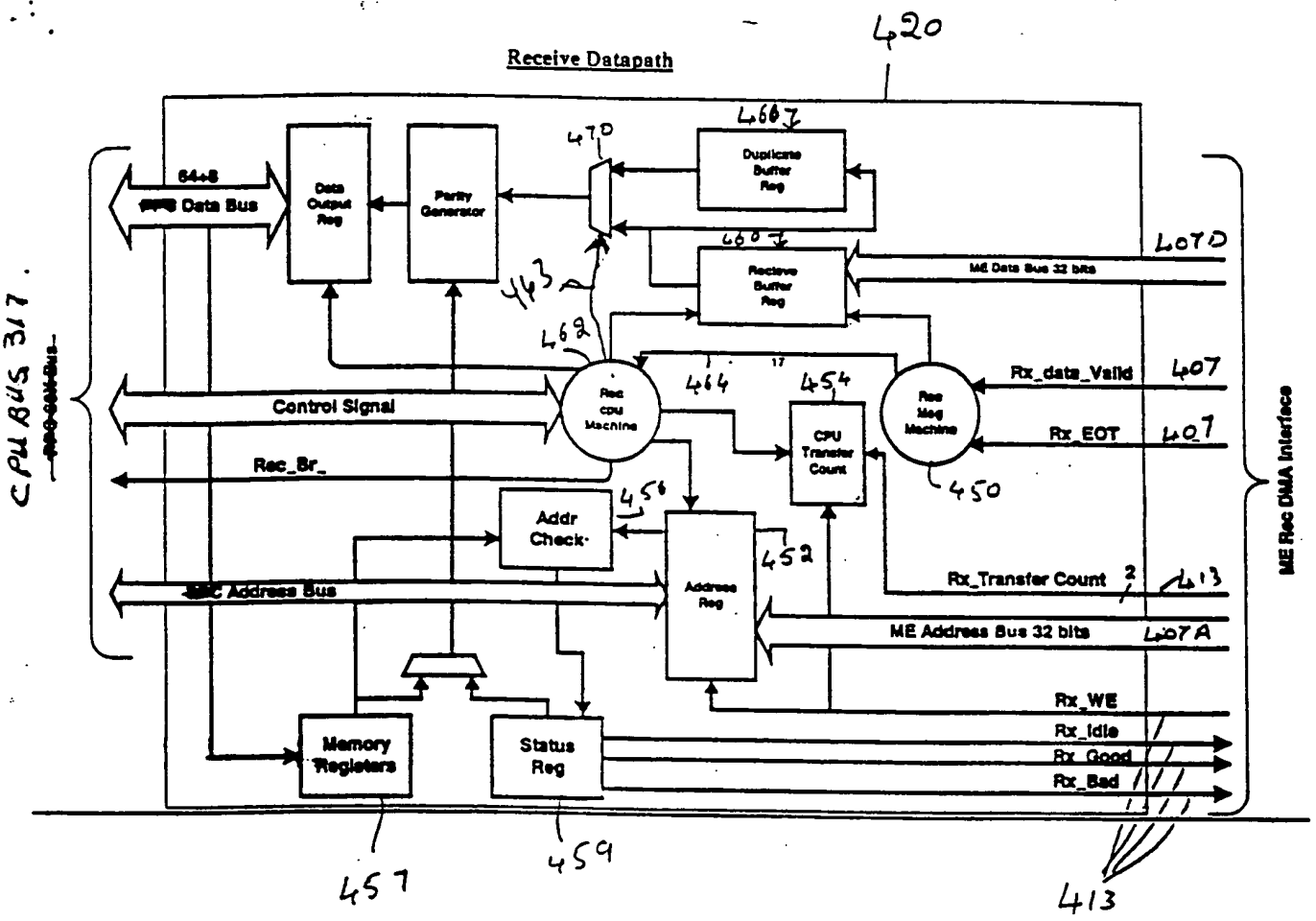

Transmit Datapath
418
415
417
421
423
409
Xmit buffer reg
Data Bus
Parity Checker
64
Data to reg
32
402
419
Xmit CPU Machine
Control Signal
427
Xmit Byte Machine
433
Tx_data_Valid
Tx_EOT
405
Xmit_Dr
Addr Reg
Parity Generator
Mem Addr Reg
437
Addr Cnt
431
CPU Transfer Count
439
Xmit Transfer Count
435
413
Addr Reg
Address Bus
32-bit
317A
Status Reg
404
Tx_WE
Tx_Addr
Tx_Cntrl
Tx_Data
411

FIG 10


420
Receive Datapath
460
Duplicate Buffer Reg
470
Data Output Reg
Parity Generator
460
Receive Buffer Reg
ME Data Bus 32 bits
405
462
463
464
454
Rec cpu Machine
Rec Msg Machine
Rx_data_Valid
407
Rx_EOT
407
Control Signal
Rec_Br_
CPU Transfer Count
450
456
Addr Check
452
Address Reg
Rx_Transfer Count
413
ME Address Bus 32 bits
407A
Rx_WE
Rx_Idle
Rx_Good
Rx_Bad
Memory Registers
Status Reg
457
459
413
CPU BUS 317
ME Rec DMA Interface

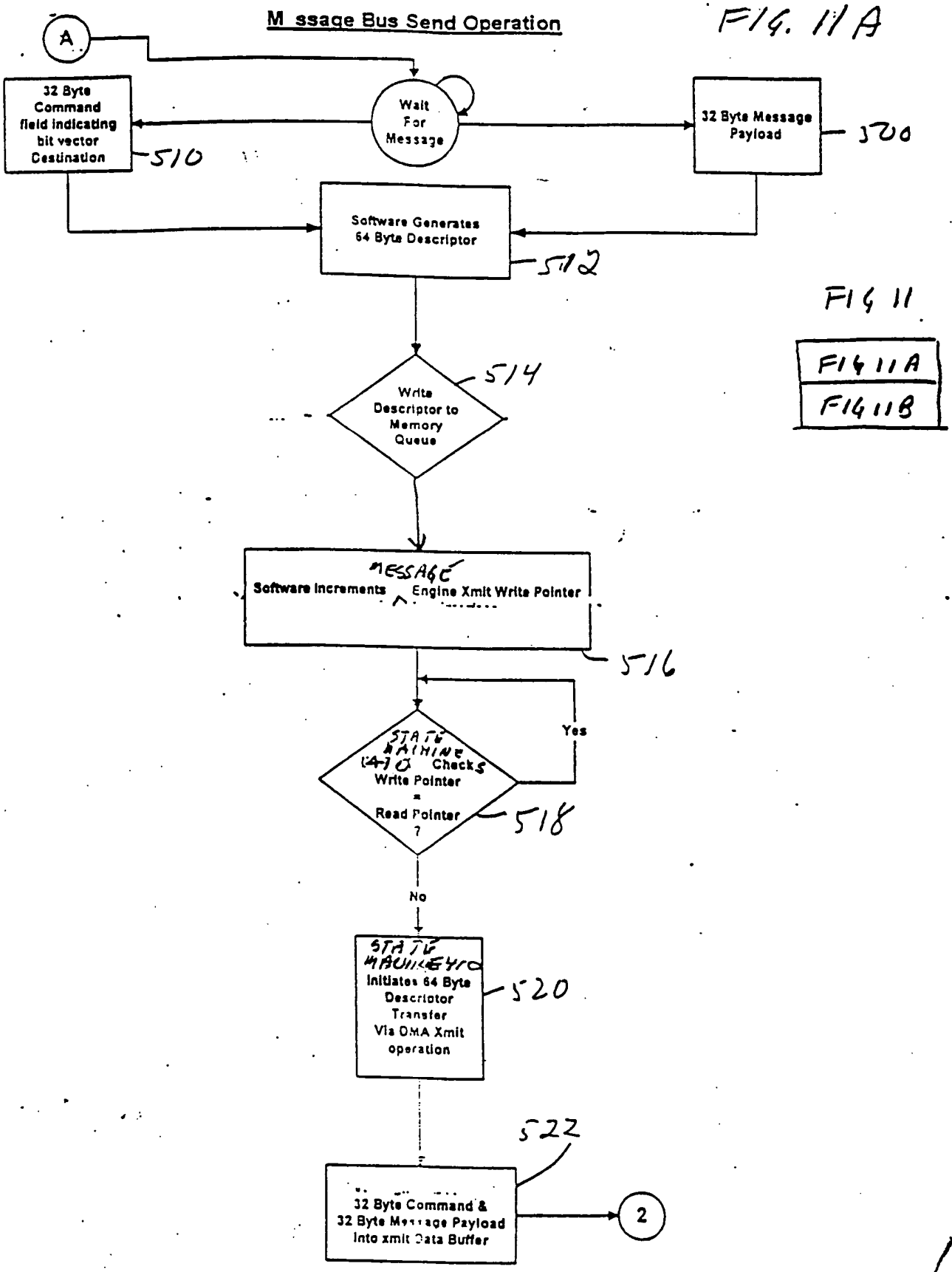


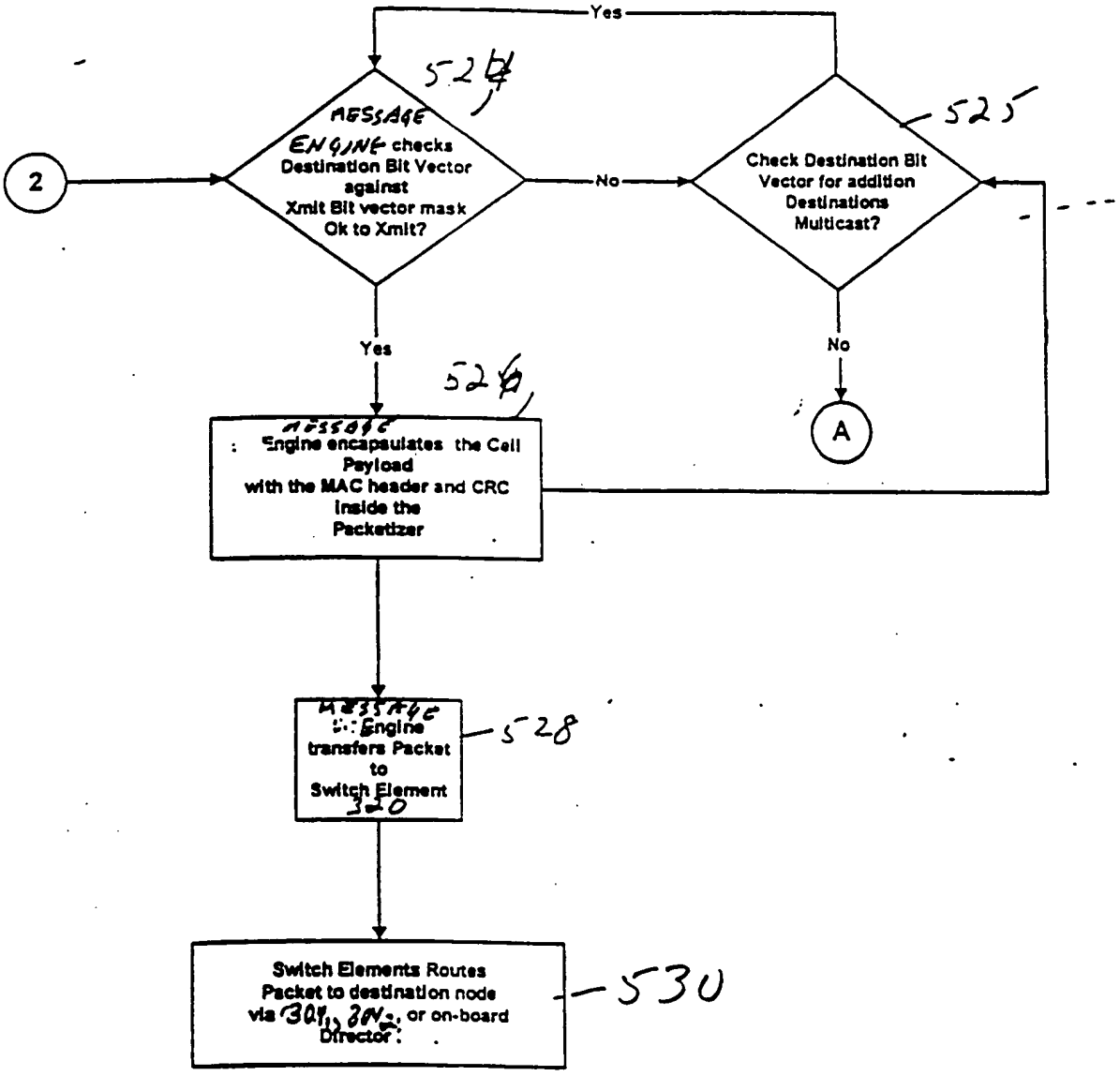
FIG. 11A

FIG 11

FIG 11A
FIG 11B

M ssage Bus Send Operation Continu d

FIG 11B



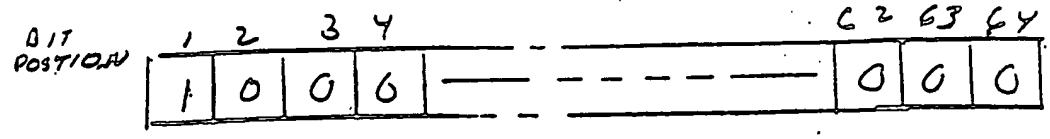


FIG 11C

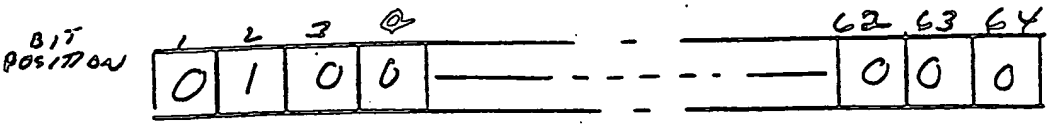


FIG 11D

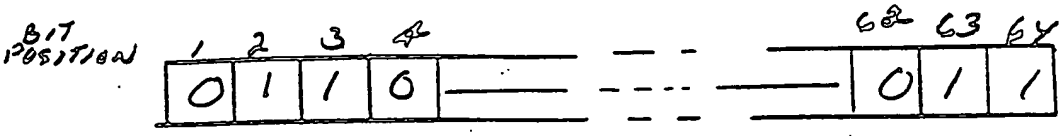


FIG 11E

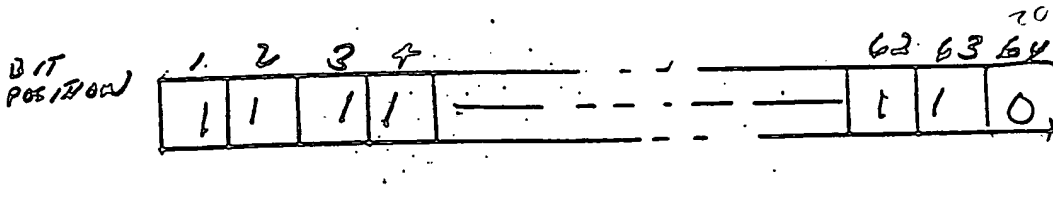


FIG 11F MPSI

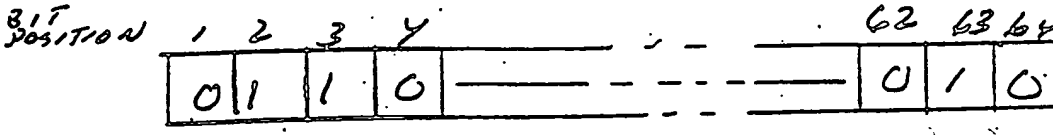


FIG 11G

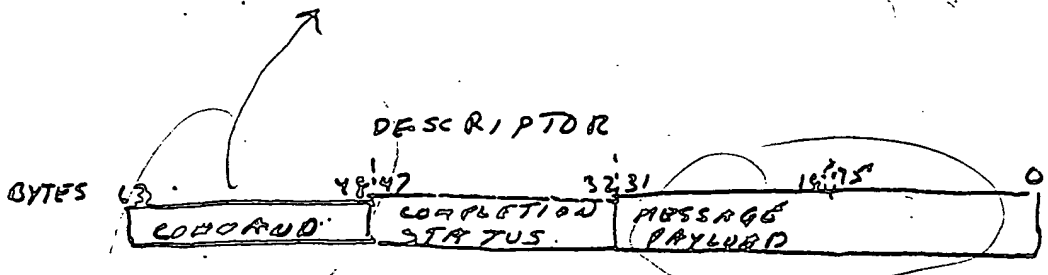


FIG 2A

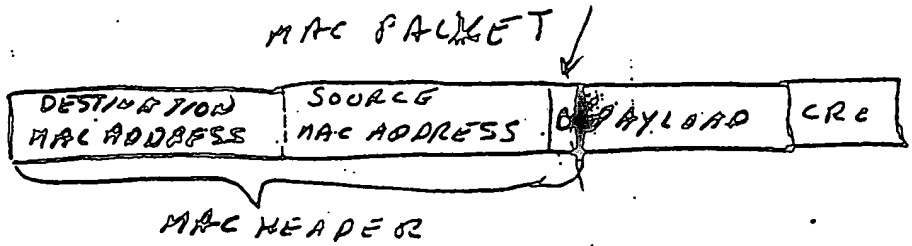


FIG 2B

Message Bus Receive Operation

FIG. 12A

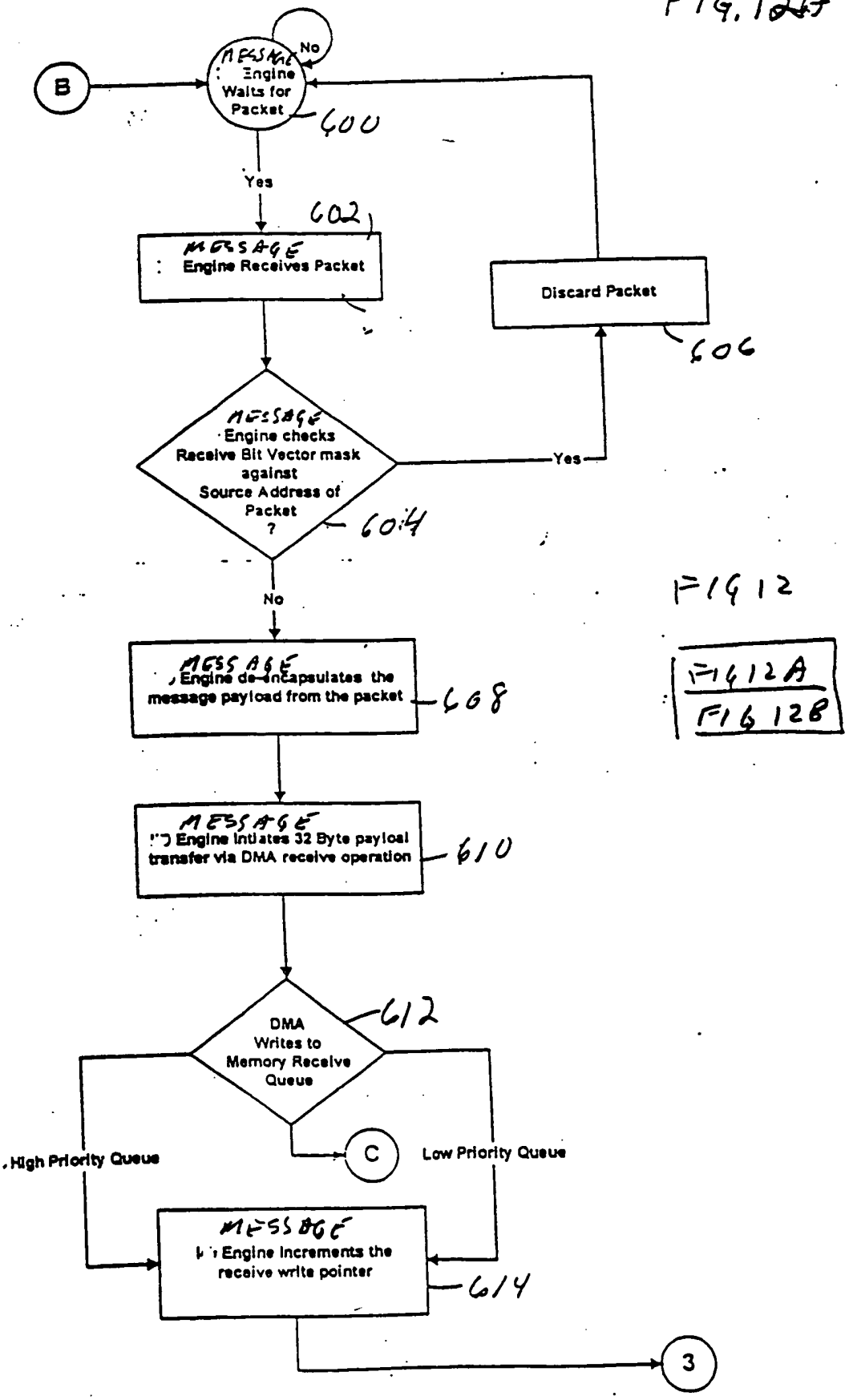


FIG 12

FIG 12A
FIG 12B

M ssage Bus Receive Operation Continued

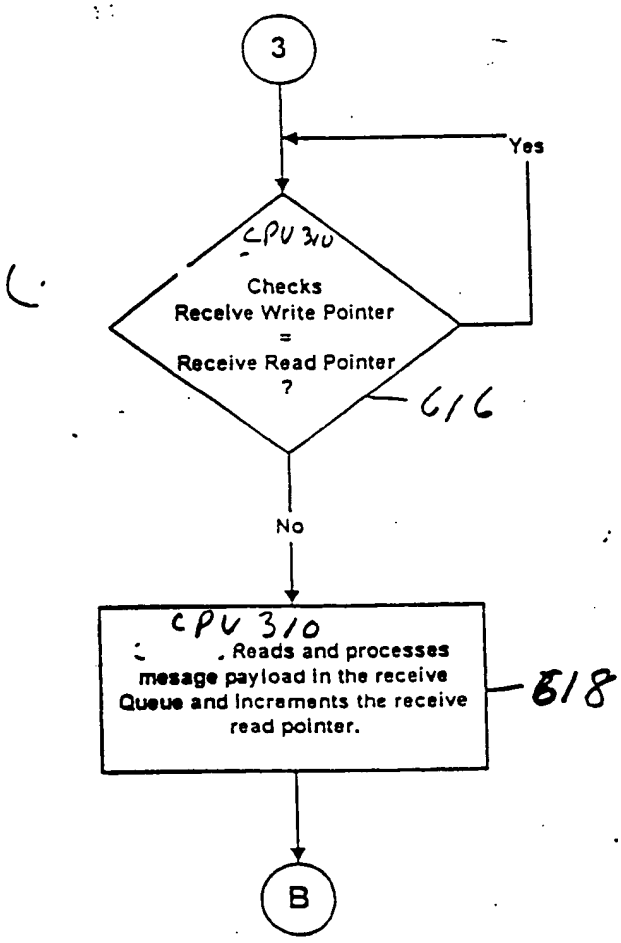


FIG 12B

Messag Bus Acknowl dgement Operati n

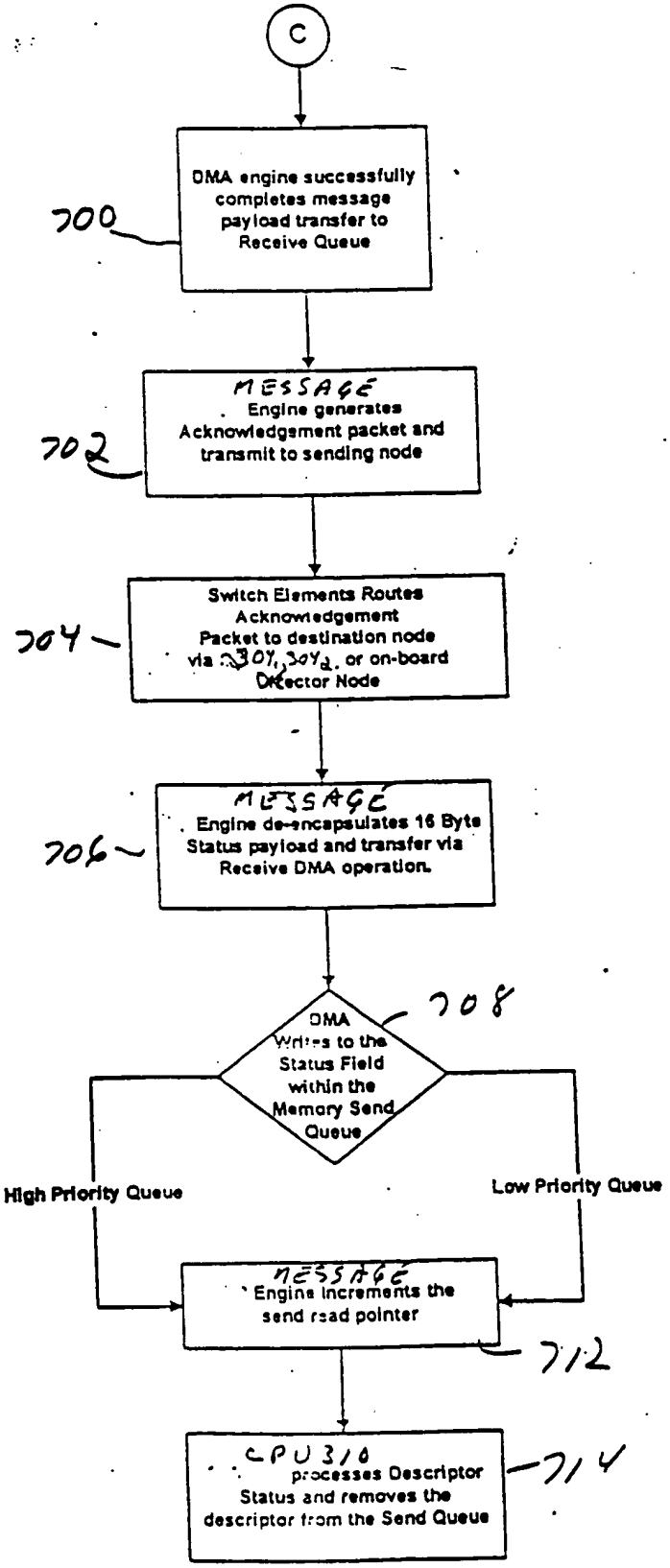
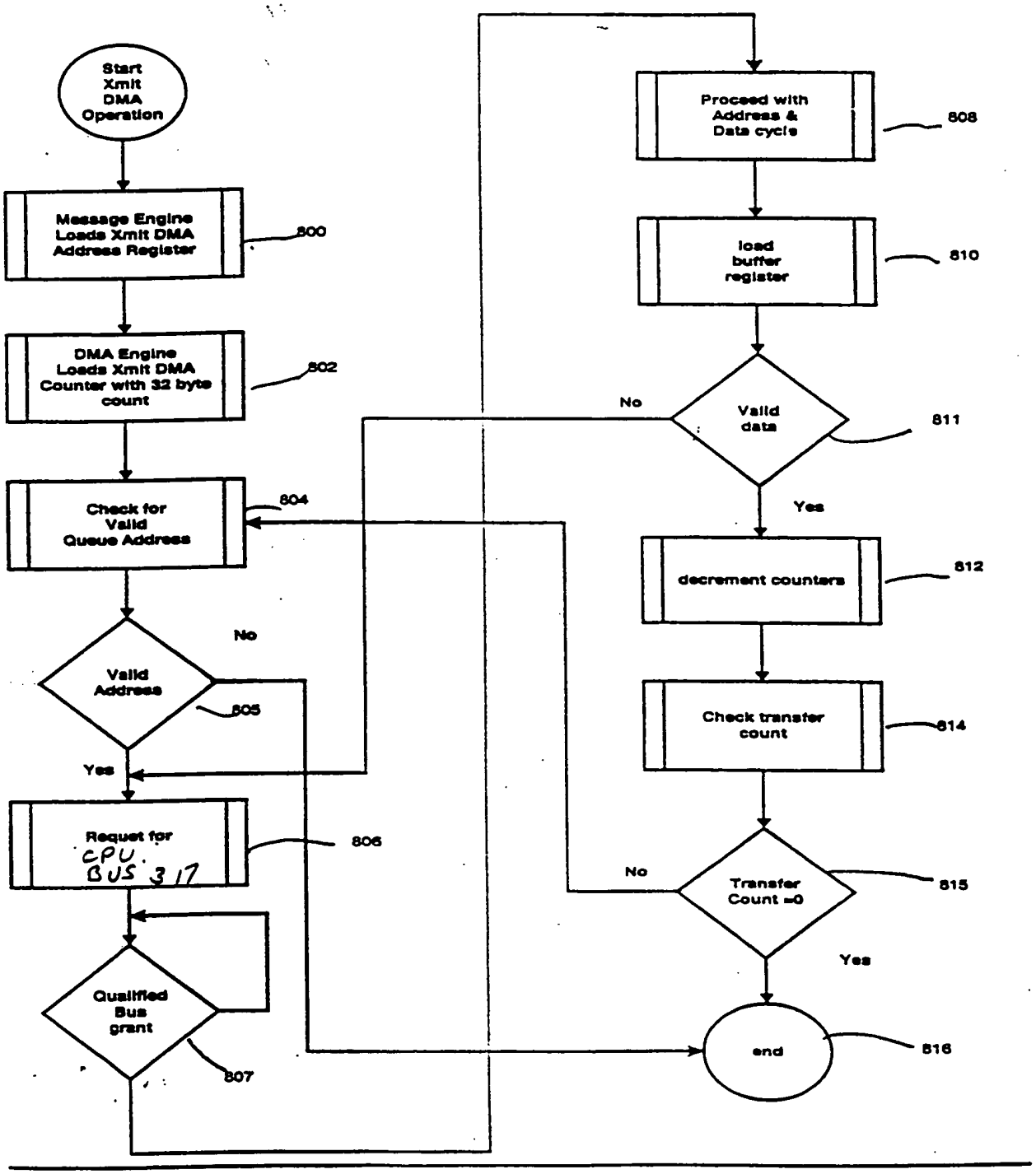


FIG. 13

FIG 14A

Xmit CPU flow



F-1414B

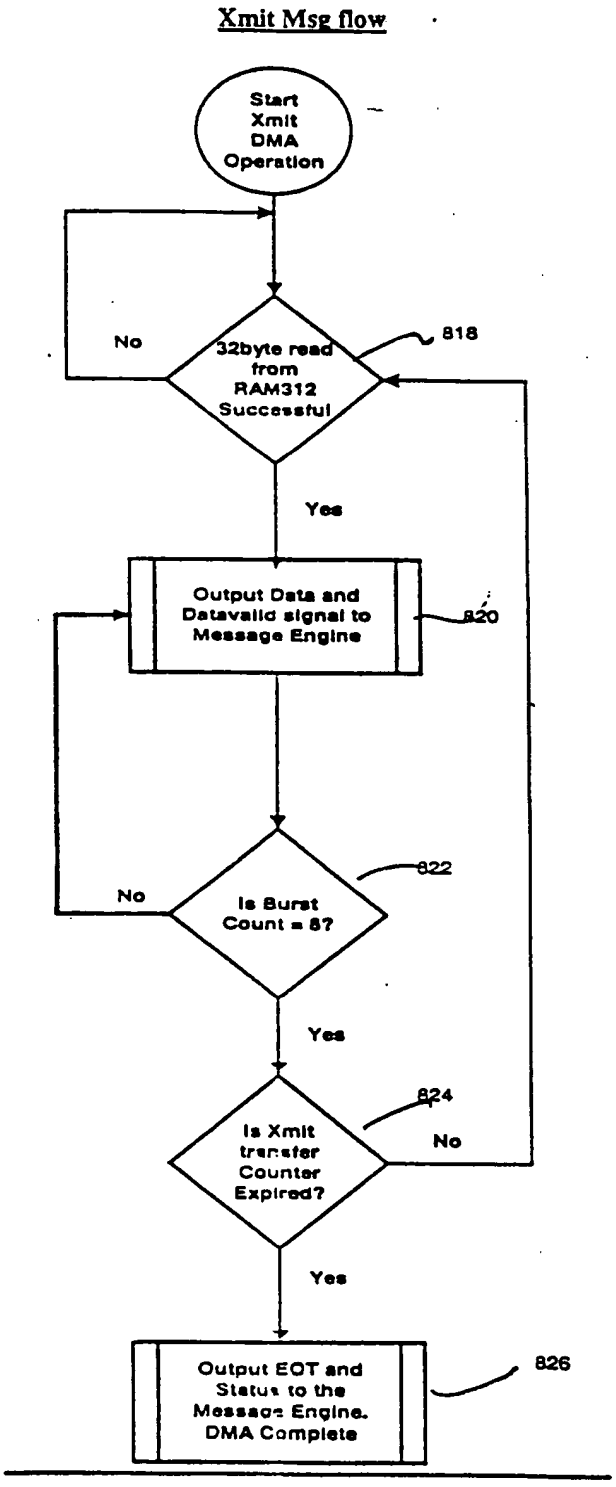

Xmit Msg flow
Start Xmit DMA Operation
32byte read from RAM312 Successful
No
818
Yes
Output Data and Datavalid signal to Message Engine
820
Is Burst Count = 8?
822
No
Yes
Is Xmit transfer Counter Expired?
824
No
Yes
Output EOT and Status to the Message Engine. DMA Complete
826

FIG 15A

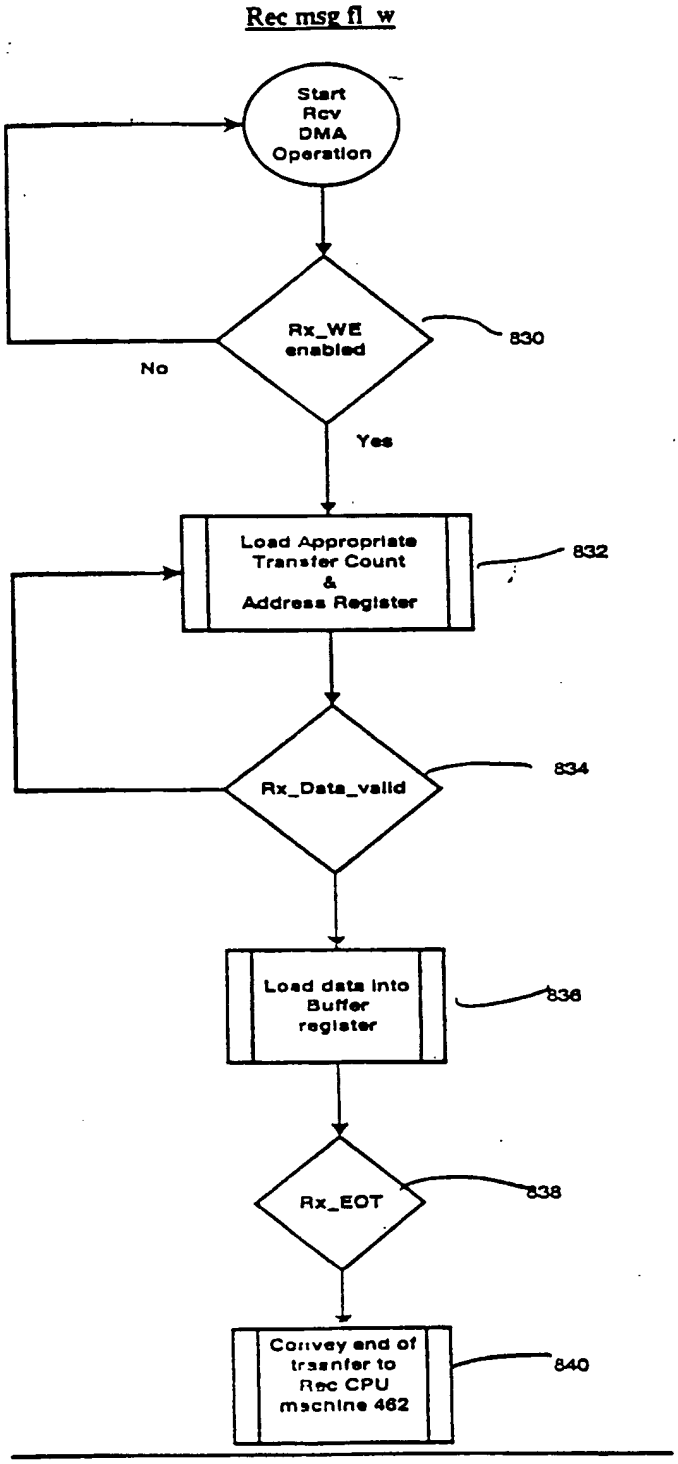

Rec msg fl w
Start Rcv DMA Operation
Rx_WE enabled
830
No
Yes
Load Appropriate Transfer Count & Address Register
832
Rx_Data_valid
834
Load data into Buffer register
836
Rx_EOT
838
Convey end of trasnfer to Rec CPU machine 462
840

FIG 15B

Rec cpu flow